15. (Original) The integrated circuit chip package of claim 14, wherein the plurality of partially captured pads are formed by a mask having elongated non-circular mask openings.

a' cont.

16. (Original) The integrated circuit chip package of claim 15, wherein the elongated non-circular mask openings have a first dimension and a second dimension.

17. (Original) The integrated circuit chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is greater than the second dimension of the elongated non-circular mask openings.

18. (Original) The integrated circuit chip package of claim 16, wherein the first dimension of the elongated non-circular mask openings is selectively oriented on the substrate in the direction of highest stress within each interconnection.

19. (Original) The integrated circuit chip package of claim 14, wherein the interconnections have a combination of mask-defined and pad-defined solder joint profiles.

20. (Amended) A substrate having a plurality of non-directional conductive pads and a mask thereon, wherein the mask has a plurality of openings having a first dimension larger than a diameter of the conductive pad, and a second dimension smaller than the diameter of the conductive pad, and wherein the first dimension is oriented in the direction of highest stress within interconnections formed within the openings of the mask.

a' cont.

21. (Original) The substrate of claim 20, wherein the conductive pads are circular.

22. (Original) The substrate of claim 20, wherein the first dimension of the openings is greater than the second dimension of the openings.

23. (Amended) The substrate of claim 22, wherein the first dimension of the openings is selectively oriented in the direction of highest stress within a plurality of interconnections formed within the openings of the mask.

24. (Amended) An integrated circuit mask having a plurality of elongated non-circular openings therein, wherein the openings have a first dimension greater than a second dimension, such that the first dimension of the openings coincides with the direction

of the highest stress within interconnections formed by the openings.

a' cancel'd.

25. (Original) The integrated circuit mask of claim 24, wherein the mask comprises a non-wettable material.

REMARKS

Claims 1-26 are pending in this application. Claims 1-13 have been withdrawn from consideration. By this amendment claims 14, 20, 23 and 24 have been amended. Reconsideration and allowance in view of the amendments and the following remarks are respectfully requested.

Claims 20-24 are rejected under 35 U.S.C. §112, first paragraph. By this amendment claims 20 and 24 have been amended for clarification. Accordingly, Applicants respectfully request withdrawal of these rejections.

Claims 20 and 24-26 are rejected under 35 U.S.C. §102(b) as being anticipated by Shirai et al. (US 5,517,756, hereinafter "Shirai"). Claims 20 and 21 are rejected under 35 U.S.C. §102(e) as being anticipated by Lee (US 5,872,399). Claims 14-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Zakel (US 6,277,660). Claims 14-19 and 21-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shirai.